WE CLAIM:

1. An apparatus comprising:

a first circuit configured to receive first data, wherein the first circuit is configured to translate the first data into PCI formatted data;

a PCI data bus;

a second circuit coupled to the first circuit via the PCI data bus, wherein the second circuit is configured to receive the PCI formatted data from the first circuit via the PCI data bus, wherein the second circuit is configured to translate the PCI formatted data received from the first circuit into PCI-Express formatted data;

wherein the PCI data bus is configured to transmit data between only the first and second circuits.

2. The apparatus of claim 1 further comprising:

a PCI-Express data bus;

a second PCI data bus;

a third circuit configured to receive third data, wherein the third circuit is configured to translate the third data into PCI formatted data;

a fourth circuit coupled to the third circuit via the second PCI data bus and coupled to the second circuit via the PCI-Express data bus, wherein the fourth circuit is configured to receive the PCI formatted data from the third circuit via the second PCI data bus, wherein the fourth circuit is configured to translate the PCI formatted data received from the third circuit into PCI-Express formatted data;

wherein the second PCI data bus is configured to transmit data between only the third and forth circuits.

3. The apparatus of claim 1 further comprising:

a PCI-Express data bus coupled to the second circuit;

a translator circuit coupled to the second circuit via the PCI-Express data bus.

4. The apparatus of claim 1 wherein the first integrated circuit, the second integrated circuit, and the PCI data bus are integrally formed on one semiconductor substrate.

5. The apparatus of claim 1 wherein the first and second circuits are formed on first and second semiconductor substrates, respectively, wherein the PCI data bus is formed on a printed circuit board.

6. An apparatus comprising:

a PCI data bus;

a first circuit coupled to the PCI data bus and configured to receive first data, wherein the first circuit is configured to process the first data for subsequent transmission over the PCI data bus;

a second circuit coupled to the first circuit via the PCI data bus, wherein the second circuit is configured to receive second data from the first circuit via the PCI data bus, wherein the second circuit is configured to process the second data for subsequent transmission over a PCI-Express bus;

wherein the PCI data bus is configured to transmit data between only the first and second circuits.

7. The apparatus of claim 6 further comprising:

the PCI-Express data bus;

a second PCI data bus;

a third circuit coupled to the second PCI data bus and configured to receive third data, wherein the third circuit is configured to process the third data for subsequent transmission over the second PCI data bus;

a fourth circuit coupled to the third circuit via the second PCI data bus, wherein the fourth circuit is configured to receive fourth data from the third circuit via the second PCI data bus, wherein the fourth circuit is configured to process the third data for subsequent transmission over the PCI-Express bus;

wherein the second PCI data bus is configured to transmit data between only the third and fourth circuits.

8. The apparatus of claim 6 further comprising:

the PCI-Express data bus coupled to the second circuit;

a translator circuit coupled to the second circuit via the PCI-Express data bus.

9. The apparatus of claim 6 wherein the first integrated circuit, the second integrated circuit, and the PCI data bus are integrally formed on one semiconductor substrate.

10. The apparatus of claim 6 wherein the first and second circuits are formed on first and second semiconductor substrates, respectively, wherein the PCI data bus is formed on a printed circuit board.

11. A system comprising:

a first pair of circuits;

a second pair of circuits;

a first PCI data bus, wherein the first PCI data bus transmits data between the first pair of circuits;

a second PCI data bus, wherein the second PCI data bus transmits data between the second pair of circuits;

first and second PCI-Express data buses coupled to one circuit of the first pair and one circuit of the second pair, respectively.

12. The system of claim 11 wherein the first pair of circuits and the first PCI data bus are integrally formed on one semiconductor substrate.

13. The system of claim 11 wherein the first pair of circuits are formed on respective semiconductor substrates, and wherein the PCI data bus is formed on a printed circuit board.

14. The system of claim 11 wherein the first PCI data bus transmits data only between the first pair of circuits, and wherein the second PCI data bus transmits data only between the second pair of circuits.

15. An apparatus comprising:

a PCI data bus;

a first circuit;

a second circuit, wherein the second circuit is configured to transmit data to a PCI-Express bus;

wherein the PCI data bus transmits data only between the first and second circuits.